IN THE CLAIMS:

Claims 10-29 were previously withdrawn and have been canceled herein for the filing of a divisional patent application. None of the pending claims 1-9 have been amended herein. All of the pending claims 1-9 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

1. (Previously Presented) A threshold-adjusted transistor, comprising:
a substrate including:
spaced-apart source and drain regions formed in the substrate; and
a channel region defined between the source and drain regions;
a layer of gate oxide formed over at least a part of the channel region; and
a gate formed over the layer of gate oxide, the gate further having at least one implant aperture formed therein, the channel region of the substrate further including a channel internal implanted region between the source and drain regions, the source and drain regions each including lightly doped extensions under the gate and the lightly doped extensions and the channel internal implanted region being substantially equivalently doped.

2. (Original) The transistor of claim 1, the substrate further comprising at least one lightly-doped structure located between at least one of the source and drain region and the channel region.

3. (Original) The transistor of claim 2, further comprising a double-diffused structure at least partially surrounding each of the channel internal implanted region and the at least one lightly-doped structure.

4. (Previously Presented) The transistor of claim 3, wherein the double-diffused structure is implanted at a diagonal angle to the gate and through the at least one implant aperture of the gate.

5. (Original) The transistor of claim 1, the substrate further comprising an enhancement region located within at least a portion of the channel region.

6. (Previously Presented) The transistor of claim 2, wherein the channel internal implanted region and the at least one lightly-doped structure are formed according to the same fabrication process.

7. (Previously Presented) The transistor of claim 2, wherein the at least one lightly-doped structure is a lightly-doped drain (LDD) structure arranged between one of the drain and source regions and the channel region.

8. (Original) The transistor of claim 1, wherein the at least one implant aperture comprises a plurality of implant apertures arranged in a checkerboard configuration along the gate.

9. (Original) The transistor of claim 1, wherein the at least one implant aperture comprises a plurality of implant apertures arranged in a two dimensional array configuration along the gate.

10-29. (Canceled).